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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,935	02/20/2004	David C. McClure	28940-00172USPT	7267

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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,935	MCCLURE, DAVID C.	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. **The applicant's abstract fails to meet these requirements, as it contains fewer than 50 words and fails to describe the disclosure sufficiently to the reader.**

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent Publication to Seki et al (US 2002/0016914 A1).

4. **Regarding claim 1,** Fig. 12 of Seki discloses a volatile memory array (**12E**), a logic circuit operable to detect a tamper situation and generate at least one control signal responsive thereto (**604**), and circuitry associated with each of a plurality of memory cells in the volatile memory array which responds to the control signal and destroys the data stored in the associated memory cell (see paragraphs 0111 and 0112).

5. **Regarding claim 2,** Fig. 12 discloses all the claimed elements above comprising a smart card. In Fig. 2 of the present application, the applicant discloses a smart card (**30**) that includes a power source (**34**), a logic circuit to detect a tamper situation (36), and a volatile memory array (**32**). As mentioned above, Fig. 12 of Seki discloses a device (600) that includes a power source (**601, 602**), a logic circuit to detect a tamper situation (**604**), and a volatile memory array (**12E**).

6. Claims 9-11, 14-18, 21-22, 25, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent Publication to Sakata (5,781,482).

7. **Regarding claims 9-11, 14-18, 21-22, 25, and 28,** Sakata teaches, in Fig. 1, a data latch having a true node and a complement node, and circuitry responsive to control signals to short the true node to the complement node for the purpose of destroying data stored by the latch. This circuitry comprises p-channel transistors and n-channel transistors (**201, 203, 205, 207**) having the gates connected to receive a control signal (**φ or φ_1**). When the SRAM is in reset mode, lines R_1 and R_2 are grounded or shorted, and the data is destroyed (column 2, lines 49-55).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent Publication to Seki et al (US 2002/0016914 A1) in view of the US Patent to Murray (6,469,930).

10. **Regarding claims 3-6,** Seki teaches all the claimed elements, but fails to teach that the cells comprise 6T cells in the form of a data latch, in which the latch nodes and bit lines are driven to a reference voltage. Murray discloses, in Fig. 3A-B, a data latch (**102**) comprised of a 6T type cell (**106-112**), in which the latch nodes and bit lines (**BL, BLB**) are driven to a reference voltage. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data latch structure of Murray in the device of Seki because this type of 6T latch structure is well-known as prior art, as disclosed by the applicant (Fig. 1).

11. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent Publication to Seki et al (US 2002/0016914 A1) in view of the US Patent to Sakata (5,781,482).

12. **Regarding claims 7-8,** Seki teaches all the claimed elements, but fails to teach circuitry that unbalances the data latch and exercises unique reference voltage control over each side of the latch. Sakata discloses, in Fig. 1, a switch (**200**) that unbalances the latch (**100**) in response to control signals φ and φ_1, which in turn controls set/reset lines S_1, S_2, R_1, and R_2, which apply unique reference voltages over each side of the latch, which can reset or destroy the data stored therein. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the switch of

Sakata to perform this same function, namely the resetting of the latch and the destruction of data, in the system of Seki.

13. Claims 12-13, 19-20, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakata (5,781,482) in view of the US Patent to Murray (6,469,930), and further in view of Itoh et al (5,668,770).

14. **Regarding claims 12-13, 19-20, and 29-30,** Sakata teaches all the claimed elements as discussed above, but fails to teach first and second pass gates coupling true and complement nodes to bit lines, and circuitry to disconnect a voltage line from a latch upon receipt of a control signal. Murray teaches, in Fig. 3A-B, a data latch having a true node and a complement node (**114, 116**), and a first pass gate coupling the true node to a bit line (**118**), and a second pass gate coupling the complement node to a complement bit line (**120**). Itoh teaches, in Fig. 1A, a circuit that acts as a switch (Q_P) to ground a voltage when the logic circuit generates a control signal (φ_P). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the circuitry of Itoh, which disconnects a reference voltage line from the latch when a control signal is activated, with the system of Sakata to short the true and complement nodes to a reference voltage for the purpose of destroying data stored by the latch.

15. Claims 23-24, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakata (5,781,482) in view of the US Patent to Matsui et al (5,276,647).

16. **Regarding claims 23-24 and 26-27,** Matsui teaches (column 12, lines 52-58) a circuit that uses the same control signal and different control signals to do the do the same task. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the circuitry of Hirose, which would reset or destroy data by shorting the true and complement nodes, with the circuitry of Sakata, which comprises a p-channel transistor and an n-channel transistor responsive to control signals, and control it with the same or different control signals taught by Matsui. This circuitry could then be used in the system of Sakata to short the true and complement nodes to a reference voltage for the purpose of destroying data stored by the latch.

17. Claims 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Sakata (5,781,482) in view of the US Patent to Yanagisawa (5,226,011).

18. **Regarding claims 31-34,** Sakata teaches all the claimed elements as discussed above but fails to teach that each side of the latch has a separate positive reference voltage input, and that NOT logic gates comprise the circuitry that couples each side of the latch to a voltage supply in order to destroy the data in the latch. Yanagisawa teaches, in Fig. 5, two sides of a latch comprised of transistors (Q10, Q11, Q12, Q13) associated with two reference voltages. Yanagisawa also teaches (column 6, lines 49-56; column 8, lines 30-32) the use of NOT logic gates (N4, N6) to switch levels from low to high, and vice versa, similar to the way the NOT gates in the present application are used. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the separate reference voltages and the NOT gates of

Yanagisawa with the system of Murray for the purpose of destroying data stored by the latch.

19. Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Murray (6,469,930) in view of the US Patent to Casper et al (6,041,003), and further in view of the US Patent to Brady (6,157,578).

20. **Regarding claims 35-39,** Murray teaches all the claimed elements, but fails to teach circuitry that shorts a bit line to a reference voltage. Murray also fails to teach circuitry that shorts a bit line to a word line to share charge there between, and a pull-up device to pull the word line up to a positive reference voltage after charge has been shared between the bit line and word line. Casper discusses the occurrence of a word line shorted to a bit line, and explains how this has the same effect as shorting the bit line to a ground potential, which is a reference voltage. Casper also discusses a device that restores, or pulls up, the bit line to an equilibrium voltage level. Brady discusses a device (**30**) that pulls up bit lines (**21,22**) and word lines (**24**) to two separate positive reference voltages V_{ss} and V_{dd}. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Casper and Brady, namely shorting a bit line to a word line or a reference voltage and pulling the lines up to a positive voltage level after charge has been shared, and use them in the system of Murray for the purpose of destroying data stored by the latch.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
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